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IPC-9201A

Surface Insulation Resistance Handbook

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3000 Lakeside Drive, Suite 309S, Bannockburn, IL 60015-1249
Tel. 847.615.7100 Fax 847.615.7105
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Surface Insulation Resistance Handbook

Developed by the Surface Insulation Resistance Task Group (5-32b) of the Cleaning and Coating Committee (30) of IPC

Supersedes:
IPC-9201 - July 1996

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105

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Acknowledgment

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Cleaning and Coating Committee

Chair
Douglas O. Pauls
Rockwell Collins

Vice-Chair
Debra L. Obitz
Trace Laboratories-East

Surface Insulation Resistance Task Group

Chair
Chris Mahanna
Robisan Laboratory Inc.

Technical Liaisons of the IPC Board of Directors

Peter Bigelow
IMI Inc.

Sammy Yi
Flextronics International

Surface Insulation Resistance Task Group

David C. Adams, Rockwell Collins

Allan Beikmohamadi, E. I. du Pont de Nemours and Co.

Paul A. Berry, P.E., Dow Corning Corporation

Gerald Leslie Bogert, Bechtel Plant Machinery, Inc.

Rick Carlson, Taiyo America Inc.

Beverley Christian, Ph.D., Research In Motion Limited

Gordon Davy, Northrop Grumman Corporation

Thomas G. Farrell, Underwriters Labs Inc.

Dennis Fritz, MacDermid, Inc.

Susan S.Hott, Robisan Laboratory Inc.

Christopher Hunt, Ph.D., National Physical Laboratory

Prakash Kapadia, Celestica International Inc.

William G. Kenyon, Global Centre Consulting

Jason Koch, Robisan Laboratory Inc.

Renee J. Michalkiewicz, Trace Laboratories - East

Graham Naisbitt, Gen3 Systems Limited

Beverly Newton, Dionex Corporation

Bob Neves, Microtek Laboratories

Jan Obrzut, Ph.D., NIST

John M. Radman, Trace Laboratories - Denver

Abdul Rauf, ASR Instruments, Inc.

John H. Rohlfing, Delphi Electronics and Safety

Henry Sanftleben, Delphi Electronics and Safety

Karl A. Sauter, Sun Microsystems Inc.

Russell S. Shepherd, Microtek Laboratories

Lowell Sherman, Defense Supply Center Columbus

Hans L. Shin, Pacific Testing Laboratories, Inc.

Karen A. Tellefsen, Ph.D., Alpha, Cookson Electronics

Brian J. Toleno, Ph.D., Henkel Corporation

Crystal E. Vanderpan, Underwriters Laboratories Inc.

David A. Vaughan, Taiyo America, Inc.

George Wilkish, M/A-COM Inc.

Vicka White, Honeywell Inc.

Dewey Whittaker, Honeywell Inc.

Philip W. Wittmer, Delphi Electronics and Safety

Lamar Young, Specialty Coating Systems Inc.

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Surface Insulation Resistance Handbook

1 SCOPE AND DESIGNATION

Surface Insulation Resistance (SIR) testing has been with the electronics industry since the advent of the transistor and the printed board. It has been used as a tool for incoming inspection, materials investigations and qualifications, quality conformance, prediction of long-term failure mechanisms and as a predictive tool for estimated service life.

SIR testing is a quantitative and not qualitative test method and should be viewed as an essential tool that requires understanding in order to use properly.

Electrochemical reactions at or below the surface of electronic circuits will affect their SIR. These reactions require the presence of humidity, electrical bias and ionic contaminants. The VENN diagram shown in Figure 1-1 illustrates how these reactions may be influenced.

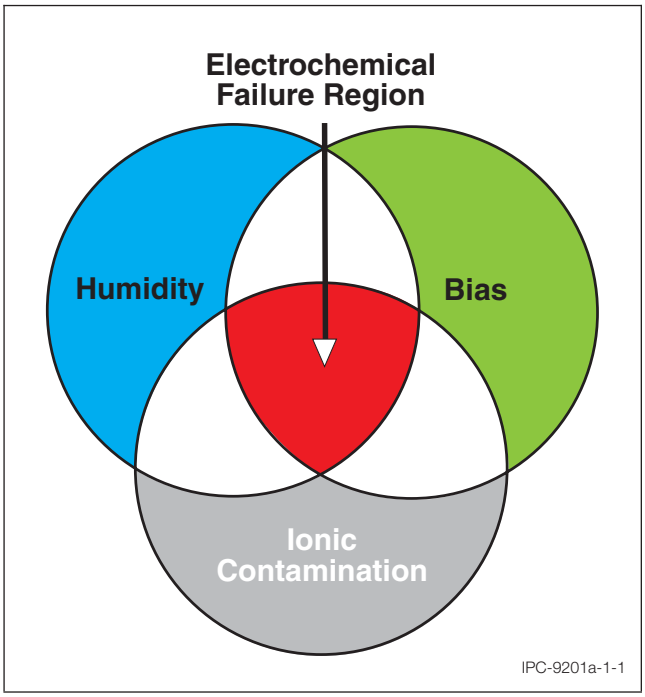

Figure 1-1 VENN Diagram Illustrating Variables Affecting Electrochemical Failure

Historically, SIR testing has been the subject of much technical argumentation; however recent science research has highlighted several significant issues that now demand modification to both this document and prevailing specifications. In particular, these are:

- Test conditions should be 40 °C, 93% Relative Humidity (RH) for no-clean regimes and 85 °C, 85% RH for other regimes.
- SIR Measurements should be taken at 20 minute intervals.
- The test voltage should be 5V.
- Voltage Gradient: 25V/mm.
- The test patterns should be 200 µm [0.0079 in] spacings and 400 µm [0.016 in] width.
- New Coupons should be employed for:
  Materials Characterization Testing.
- Process Characterization Testing.
- Current limiting resistors should be used by the measurement system so as to preserve any electrochemical reactions (dendrite formations) to aid any further analysis.

Furthermore, and resulting from the same research program, SIR can now be employed for process characterization as well as materials characterization testing.

The IPC 5-32b SIR Task Group was formed to undertake a mission of education and technical refinement of this testing into a better, more accurate and predictive tool.

1.1 Scope This document is intended to cover the broad spectrum of temperature-humidity (TH) testing, associated terminology, and suggested techniques for proper testing. This edition of the IPC-9201 has been revised in an attempt to reflect all international test specifications such as IEC and ISO.

1.2 Purpose The purpose of this document is to educate individuals who must deal with TH or temperature-humidity-bias (THB) testing. The target audience for this work ranges from the technicians running the test to engineers who must interpret the data, and those individuals responsible for specifications and standards that may call out these tests.

The guidance presented here represents the experience and technical input from many of the most knowledgeable testers in the IPC, and incorporates much of the science research that has been carried out since the document was first published. Although this handbook does not go into great depth on the underlying physics of many of the mechanisms found in SIR testing, there are references at the back of this document that may be helpful to those requiring substantiation of the issues involved.

TH and THB testing may also be related to other forms of testing, such as noise factor, corrosion testing, determination of bandwidth, characteristic impedance, etc.

1.3 How is SIR Testing Used? There are two ways in which this protocol may be used. The traditional use is in

the characterization testing of certain electronic production process chemistries such as solder masks, soldering flux, paste and wire, and conformal coatings. More recently, its use has been extended into process characterization testing, whereby the synergistic influences in the form of electrochemical reactions at each of the electronic assembly production process stages may be examined.

In general, TH or THB testing is done to show evidence of the loss of integrity or reliability in a materials system. Loss of integrity may include conformal coating or solder mask adhesion failure (less protection from the environment), decreases in dielectric strength, electrolytic corrosion, or electrochemical migration. Each of these may represent shortcomings in materials, manufacturing methods, or a susceptibility to a particular failure mechanism, which would not be desirable in the end product.

Various profiles are used to test specific failure mechanisms. The choice of cyclical or static environments, high temperature/humidity environments depends on what failure modes you are examining. Cyclical tests or TH tests examine materials properties and are often used to simulate an end-use storage environment. High-temperature/humidity tests are most often used to test for electrochemical migration or electrochemical corrosion. The high-temperature/humidity tests are also used to artificially age a materials system, simulating years of service by days of testing, in order to gain an estimate of the long-term service life of a product.

2 APPLICABLE DOCUMENTS

2.1 IPC[1]

IPC-A-24-G-KIT Surface Insulation Resistance - Gerber - KIT[2]

IPC-A-36-G Cleaning Alternatives Artwork[3]

IPC-A-52-G Cleanliness and Residue Evaluation Test Board[4]

IPC-TR-476A Electrochemical Migration: Electrically Induced Failures in Printed Wiring Assemblies

IPC-TR-580 Cleaning and Cleanliness Test Program Phase 1 Test Results

IPC-2221 Generic Standard on Printed Board Design

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-TM-650 Test Methods Manual[5]

2.6.3.1 Moisture and Insulation Resistance, Polymeric Solder Masks and Conformal Coatings

2.6.3.2 Moisture and Insulation Resistance, Flexible Base Dielectric

2.6.3.3 Surface Insulation Resistance, Fluxes

2.6.3.7 Surface Insulation Resistance

2.2 Joint Industry Standards[6]

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

2.3 International Electrotechnical Commission (IEC)[7]

IEC-61189-5 Method 5E02 Surface Insulation Resistance, Assemblies

2.4 American Society for Testing and Materials (ASTM)[8]

ASTM-D-263 Standard Specification for Chrome Oxide Green Pigment

3 SURFACE INSULATION RESISTANCE

3.1 Terms and Definitions One of the greatest sources of confusion and misunderstandings related to TH or THB testing relates to the terminology surrounding the science. For the purposes of this document, the following terms are defined.

Surface Insulation Resistance (SIR) – This is a property of the material and electrode system. It represents the electrical resistance between two electrical conductors separated by some dielectric material(s). This property is loosely based on the concept of sheet resistance (see ASTM-D-263), but also contains elements of bulk conductivity, leakage through electrolytic contaminants, multiple dielectric and metallization materials and air.

Note: Historically, SIR began as a material property to be measured on the base material, regardless of the test conditions imposed on the test specimens. As time progressed, the term ''SIR testing'' began to encompass all forms of TH testing. Present day usage of the term now refers to most TH, or accelerated aging tests, as SIR testing. The

1. www.ipc.org
2. Electronic artwork packages for fabrication test boards are available at www.ipc.org/onlinestore under ''Artwork/Test Vehicles.''
3. Electronic artwork packages for fabrication test boards are available at www.ipc.org/onlinestore under ''Artwork/Test Vehicles.''
4. Electronic artwork packages for fabrication test boards are available at www.ipc.org/onlinestore under ''Artwork/Test Vehicles.''
5. Current and revised IPC Test Methods are available on the IPC Web site (www.ipc.org/html/testmethods.htm)
6. www.ipc.org
7. www.iec.ch
8. www.astm.org

terms ''SIR'' and ''TH'' or ''THB'' are often used synonymously, although the latter is consider broader and encompasses more disciplines of testing than just SIR.

Moisture Insulation Resistance (MIR) – This is another term used in many cases to describe a THB test. For the purposes of this handbook, an MIR test is the intentional testing of a materials system in an environment where condensation is likely (cyclical).

Dendrites – These are the inter-metallic growths that are a result of electrochemical reactions. Dendrites offer a lower path of resistance to electrical current that may therefore migrate undesirably, between adjacent conductors. Refer to 3.1.1 for more detailed information and important cautionary notes. Figure 3-1 provides a visual example of dendrites.

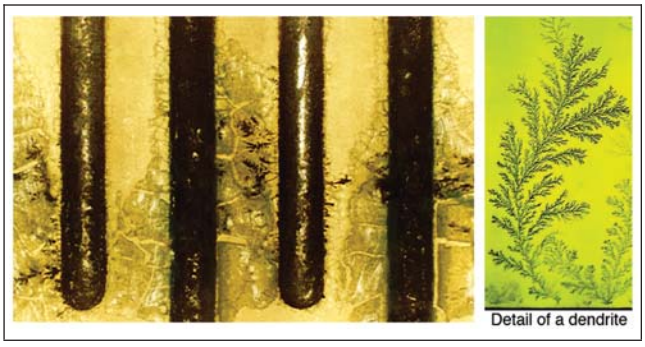

Figure 3-1 Dendrites Grown Between Oppositely Biased Conductor Lines

Materials System(s) – This refers to the entire test sample, usually consisting of two or more electrodes having various metallizations (copper or tin-lead), adhered to a dielectric surface, with some constant separation. The metal/dielectric may be covered or coated with a second polymer dielectric material, such as a solder mask or conformal coating.

Note: A tremendous number of manufacturing process variables will affect the properties of the materials system.

Relative Humidity (RH) – This refers to the amount of water vapor present in air at any temperature, relative to the total amount of water the air can hold at that temperature.

Note: An RH of 100% represents air that is saturated with water vapor. As temperature increases, the amount of water vapor that the air can hold increases. An RH of 50% at 85 °C represents far more water vapor content than an RH of 50% at 25 °C.

RH in SIR testing determines the thickness of the absorbed water surface film and, since organic materials are permeable to water molecules, the availability of moisture at internal interfaces. Below some critical RH, specific to the material system, electrochemical migration will not occur. Above this critical value, there appears to be a 10x increase in filament growth rate with every 10% rise in RH. Experimental results support the existence of an RH threshold for CAF growth below which significant filament growth was not observed (see Reference 12 in 10.1).

Conductive Anodic Filamentation or Cathodic Anodic Filamentation (CAF) – This is the growth of dendrites within the laminate or weave of a printed board. Refer to 3.1.1 for more detailed information and explanation.

Temperature-Humidity Testing (TH) – This testing regime subjects a material or material system to a set duration of temperature and humidity higher than ambient conditions, but without the application of electrical potential (voltage), except for when measurements are taken. Materials parameters (such as SIR) are measured before, during and after the test exposure.

Note: Present tests range anywhere from four days at 35 °C, 90% RH, to 56 days at 85 °C, 85% RH, depending on the intent of the test, or the specification which calls out such testing. The intent of this testing is to environmentally stress a material, and check for materials degradation.

New specifications are calling out two different conditions dependant upon the manufacturing process that the end user might adopt:

40 °C, 93% RH – This is necessary when assessing no-clean process materials, specifically solder flux

85 °C, 85% RH – This is used for all other process conditions where cleaning may be involved

The reason for the 40 °C, 93% RH method is because most no-clean flux residues begin to volatilise at temperatures above 40 °C (see Figure 3-12). If these remain on the surface, especially if conformal coatings are used, then they may well contibute to device failure, hence the need to test under ''worst-case'' conditions. In addition, this is the basis of many international standards where considerable supporting research is available.

Temperature-Humidity-Bias (THB) Testing – This testing regime subjects a material or material system to a set duration of temperature and humidity higher than ambient conditions. In addition, electrical potential is applied between adjacent electrodes of the test patterns. The level of applied potential varies, as does the duration of the potential, and the point at which the potential is applied.

Note: In present practice, the term ''electrical bias'' can refer to two different electrical potentials: electrification/measurement voltage, in which a voltage gradient is applied and the resultant currents are measured, and a non-measurement potential (bias voltage) applied to all test patterns whenever measurements are not being taken. These two terms are defined later.

***Voltage Gradient (VG)* –** The ratio of the applied voltage (expressed in volts) to the separation of electrodes (expressed in mm), e.g., 25 Volts/mm.

The VG should be the same as the finished printed board assembly. Contrary to expectation (Ohm's Law), the lower the voltage the greater the propensity for dendrite formation. See Section 4 and supporting figures.

***Electrification Voltage (EV)/Measurement Voltage (MV)/ Test Voltage (TV)* –** This is the electrical potential applied between adjacent connectors of a test pattern when measurements of resistance are made. By convention, this voltage should always be expressed as a negative number.

Note: Electrification (measurement) voltages have varied widely and evolved with advancing printed board technology. Early tests had EVs of 500 -1000 volts DC. As circuit densities increased, these levels exceeded the dielectric strength of the materials, initiating catastrophic dielectric failure. The IPC-2221 design standard limits the voltage potential between two adjacent conductors based upon the dielectric strength of the material. New research has shown that surprisingly, the lower the voltage, the greater the propensity for dendrites. See Figure 3-2 (Courtesy of the National Physical Laboratory (UK)):

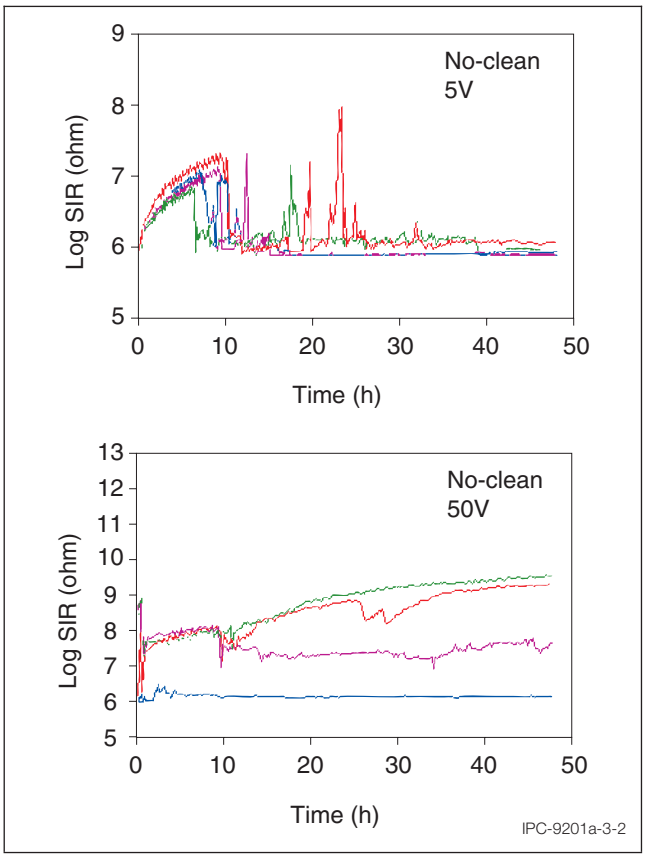

Figure 3-2 Propensity for Dendrites over Time

***Electrification Time (ET)* –** This is the amount of time that the electrification voltage is applied before the resistance measurement is recorded.

Note: Electrification time could be any amount of time, but has historically been 60 seconds due to provisions of widespread military specifications. 60 seconds has typically been a sufficient time for the system to come to equilibrium, increasing the stability of the readings. The stability of the reading can also be affected by factors such as electromagnetic interference (EMI) and triboelectric charges generated by minute movements of insulated wires. Modern available measurement equipment is designed to be able to come to equilibrium in under one second.

Also note that it is essential to avoid electrical interference, and to minimize tribo-electrical effects.

***Measurement Accuracy (MA)* –** Modern automated measurement systems are able to make readings to $<<10^{14}$ Ω. However the calibration of the measurement system is restricted to the accuracy of "known-value" resistors that is presently limited to this value.

Measuring at this pico-amperage level makes the entire measurement practice prone to false readings especially in respect to tribo-electrical interference. The quality of the cabling between the coupon under test and the measurement device is therefore critical.

Modern automated systems can now be used to make the measurements and collate the gathered data into useful SPC graphical forms.

***Bias Voltage (BV)* –** This is the electrical potential applied between adjacent connectors of a test pattern at all times when resistance measurements are not being made. When the bias voltage is opposite in polarity with respect to the measurement voltage, it is often called "reverse bias." Bias voltage is expressed as a positive number. The rationale is that this voltage is applied longer than the measurement voltage, so the BV is positive and the MV is negative. To further complicate matters, if the bias voltage and test voltage are the same polarity, both are expressed as positive values.

The level of applied bias voltage varies and has historically evolved as has electrification voltage. Original levels in both military and commercial test methods ranged from 10-100 volts DC. Bias voltage and measurement voltage should be defined by either the test method or the standard requiring the SIR test. When SIR testing is done as part of an engineering evaluation, the bias voltage should be chosen as a representative of the voltages used on the final printed board assembly. The voltage gradient should also be a consideration in that selection.

Researchers/authors define the nonmeasurement electrical potential (bias voltage) as either a positive number or a negative number, depending on the convention they use, with the test or measurement voltage as a negative or positive, respectively. In any SIR related research the reader must take care to determine which convention is being

used. Neither convention is superior to the other. The only significant difference is whether a test point becomes the cathode or the anode.

Note also that bias reversal is not a true reflection of the operating conditions on a circuit, and this test condition has been removed from modern SIR standards.

Bias Polarity (BP) – This refers to the polarity of the bias voltage relative to the electrification voltage. By convention, if the polarity of the bias voltage matches the electrification voltage, the BP is positive, otherwise the BP is negative (or reversed).

Test Duration (TD) – This refers to the length of time the materials system is exposed to conditions other than ambient conditions or controlled ambient (at test start) conditions.

Research has shown that dendrites will likely form within the first 72 hours of test, and currently there is no evidence of dendrites beginning after that time. Consequently, specifications such as IEC 61189-5 state that testing should be done for a minimum of 72 hours.

Example 1: IEC-61189-5, Test Method 5E02. In this test, a coupon is used that incorporates many typical components and has been exposed to all of the planned production processes. A VG of 25V/mm is employed using patterns that have 400 µm [0.016 in] width and 200 µm [0.0079 in] spacing. This yields a TV of 5V and measurements are made at 20-minute intervals. Automated equipment must be used for this test and the ET is therefore automatically determined by the instrument. Test duration is not less than 72 hours.

Example 2: IPC-TM-650, Method 2.6.3.1. This is a THB test, in which SIR is measured at various times. The test substrate could be an epoxy-glass laminate, with tin-lead coated test patterns, covered with solder mask, as the materials system. It is a cyclical THB test which maintains a high relative humidity throughout. An electrification voltage (EV) of +500 volts DC is used for measurements. Electrification time (ET) is 60 seconds. Bias voltage (BV) is +100 volts DC. Bias polarity is positive since the bias potential is applied in the same direction as the electrification voltage. Test duration is 168 hours or seven days.

3.1.1 Metal Migration/Filament Formation A more in-depth discussion of metal migration, dendritic growth, conductive anodic filaments, electromigration and electrochemical migration may be found in IPC-TR-476A.

The terminology surrounding the migration of metals between cathode and anode under various test conditions has been a controversial subject in past discussions in IPC subcommittees. The primary issue has been defining these tests depending on the presence/absence of water, and the form of that water, in the testing.

Solid State Electromigration (Emg) – (See Reference 14 in 10.1.) Solid state metal electromigration is in contrast to electrochemical migration (see below). Electromigration is the current induced transport of metal ions in a metal conductor. Failures or degradation of electronic devices have been observed when thin film metal conductors (e.g., aluminum, gold, copper) have been subjected to current densities in excess of 10 A/cm^2, usually at elevated temperatures. In metal electromigration, the electrons, which are conducting current, scatter off self-diffusing metallic ions and impart momentum to them causing an ion flux toward the positive end of the conductor. Failure results from a divergence of the ion flux. The location of the failure is determined by where the maximum in the divergence occurs.

The ASM Electronics Materials Handbook (Vol. 1) defines electromigration as a mechanism of mass transport under the influence of an applied direct current (DC) bias that can cause the formation of voids in certain areas of the metallization and protrusions, or ''hillocks'' in others. Electromigration occurs at high current densities. This is a different mechanism than solid state electromigration, defined above.

Note: Electromigration differs from Electrochemical migration (see below) in that EMg occurs primarily in integrated circuits under dry conditions, where EcMg occurs on printed board assemblies under liquid/electrolyte conditions. Failure occurs when the metal filament grows across or through the dielectric material to the opposing electrode.

Electrochemical Migration (EcMg) – (See Reference 14 in 10.1.) Electrochemical migration is defined as the growth of conductive metal filaments on a printed board under the influence of a DC voltage bias. This may occur at an external surface, an internal interface, or through the bulk material of a composite (e.g., paper/phenolic laminate). Growth of the metal filament is by electrodeposition from a solution containing metal ions which are dissolved from the anode, transported by the electric field and redeposited at the cathode. This definition excludes phenomena such as field induced metal transport in semiconductors and diffusion of the products arising from metallic corrosion.

There are two distinct electrochemical phenomena. In one case, surface dendrites have been known to form from the cathode to the anode under an applied voltage when a contamination is present. When the conductors are tin/lead solder, the dendrites will be lead needles which form ''tree-like'' dendrites, and lead needles coated with tin, which form ''lacy'' dendrites. If the bias voltage is sufficiently high, and the dendrite bridges between cathode and anode, an electrical short is created, often with a momentary high current flow. This current flow can cause the fragile dendrite to partially vaporize, leaving a visual formation. A related electrochemical phenomena, called conductive

anodic filament (CAF), can arise if the bias voltage is great enough. Dendritic growth is a surface effect where CAF occurs primarily in the glass bundles of the substrate laminate material.

When a material or material system is tested in a humid environment, the water vapor can combine with ionic or inorganic contaminants, producing electrolytic solutions. Metals then migrate from anode to cathode across the surface of a material using the electrolytic solution as the carrier for the mobile ions. This is essentially a microscopic plating cell. The rate at which the EcMg occurs depends on the pH of the electrolyte, the ionic mobility of the ions, the anode-cathode spacing, the metals involved, and the magnitude of the electrical potential. EcMg testing is typically done at voltages ranging from 10 to 100 volts DC.

It is intended that EcMg specifically be related to the movement of metal ions creating filaments. If an electrolytic solution is present, ions (such as chloride) can flow from cathode to anode, creating electrical leakage currents, but not necessarily metal migration. In SIR testing, it is not typically possible to separate leakage currents due to metal ion movement from leakage caused by nonmetal movement.

CAF differs from the surface dendritic growth, described above, in three ways:

(1) The migrating metal is copper, not lead or tin.

(2) The filament growth is from anode to cathode.

(3) The filament is composed of a metallic salt, not neutral metal atoms.

In CAF growth, the copper base metal under the tin/lead solder is the source of the metallic ions which are electrochemically produced at the anode and migrate along the glass-resin interface. The most common anion observed in CAF growth is chloride (as determined by SEM/EDX), although bromide ions have also been observed. A model has been developed of the dependence of failure rate on temperature, relative humidity, and voltage (see Reference 11 in 10.1). CAF formation has been observed with voltages as low as 50 volts DC.

Electromigration Testing (EMg) – This is the testing of a material or material system using an applied electrical potential, ambient or elevated temperature, in a dry (RH<< 10%) environment.

Electrochemical Migration Testing – This is the testing of a material or material system using elevated temperatures, an applied electrical potential, and water vapor. This kind of testing is generally applied to solid state devices, sometimes in bare die form and sometimes encapsulated.

Note: It is generally agreed that the deposition of liquid water (not water vapor or steam), either by condensation on the test sample or by airborne water droplets, will invalidate this testing if the electrical test patterns are not protected by a polymer coating such as solder mask or conformal coating.

Rain Forest Test – This type of testing was developed by Dr. Jack Brous, Alpha Metals, and is a form of EcMg testing. A sample-loaded chamber is taken to a high temperature and humidity (near saturation), then shut off. Since the system is sealed, as the air cools, the temperature drops past the dew point, and liquid water will begin to condense on all surfaces in the chamber, including test samples. As all samples are electrically energized, dendritic growth will usually occur.

Dendrites – Defined in 3.1, this term applies to EcMg testing. Carbon tracks, often caused when the metal filaments conduct too much electricity and carbonize the board surface, are also sometimes mistakenly referred to as dendrites. Be aware that the term ‘‘dendrite’’ has a different meaning in metallurgical applications: A dendrite in metallurgy is a characteristic tree-like structure of crystals growing as molten metal freezes, the shape produced by faster growth along energetically favorable crystallographic directions. This dendritic growth has large consequences in regards to material properties.

Water Drop Test – This refers to a test where an electrical potential is placed on two adjacent unprotected metal patterns at ambient conditions. A drop of deionized water is then placed on the sample, bridging the two conductors. The leakage current is monitored, with the test running to failure.

Note: Pure deionized water is a poor conductor, since it has few charge carrying ions. If the test sample has contaminant materials, the DI water will tend to dissolve the contaminant, forming an electrolytic solution. The electrolytic solution then promotes leakage currents, and the electrochemical migration begins. In addition, carbon dioxide (CO_2) in the air can dissolve in the deionized water, forming ions which increase leakage currents.

3.1.2 Electrochemical Corrosion Most people are familiar with the concept of corrosion and oxidation, especially in the ‘‘snow belt’’ of the United States, where road salt corrodes the steel of cars. In these cases, an acidic solution is formed which dissolves the metal locally and combines the metal with oxygen to form an oxide, or with a surface contaminant to form a chemical salt. This occurs without the presence of electricity. The same thing, on a microscopic scale, can happen on a printed board. In this case, the presence of electricity can accelerate the corrosion mechanism. Figure 3-3 provides an example of electrochemical corrosion on a printed board.

Fluxes can contain harmful materials, such as halides or organic acids. Flux residues can dissolve in water, forming a weak electrolytic solution. Such solutions are often acidic in nature. The higher the amount of harmful residue, the

Figure 3-3 Example of Electrochemical Corrosion

greater the rate of attack on the metal of the circuit. An analogous situation would be the slow rate of corrosion of a weak acid, where the amount of harmful residue is small, compared to the fast rate of corrosion of a strong acid, where the amount of harmful residue is large.

In general, electrolytic solutions are only weakly ionic/acidic, and so it would take a long time, if left alone, for the solution to seriously affect the metal. The presence of an electrical potential can greatly accelerate the process. Much as a standard plating process is used to apply a metal surface to a substrate under the influence of electricity, an applied potential can cause a reverse plating operation (electropolishing). Copper or tin-lead can become ions in solution, leading to filament growth, or the metals can combine with surface residues, forming salts like copper chloride or copper sulfate.

If the solution is in contact with dissimilar metals, which are electrically connected (e.g., the boundary between a gold plated connector and copper or solder), an electrical cell is formed. The resultant current can provoke spontaneous corrosion.

3.2 Basic Concepts

3.2.1 Sheet Resistance Sheet resistance refers to the resistance to an electrical current by a homogenous sheet of material (very thin). The nominal resistance is equal to the resistivity of the material times the length or separation, divided by the cross sectional area:

$$R = \rho * L / A$$

Where ρ = resistivity,
A = cross-sectional area, and L = length.

Figure 3-4 shows the application of this formula when used to calculate the sheet resistance of a thin film of an insulating material. In this case, the cross sectional area is W*t. The formula then becomes:

$$R_{sheet} = (\rho_{insulator} * L) / (W * t)$$

Figure 3-5 shows the application of this formula when used to calculate the resistance of a metallic conductor. In this case, the cross sectional area is again W * t and the formula becomes:

$$R_{conductor} = (\rho_{conductor} * L) / (W * t)$$

Example: Two conductors, each 100 mm long (L), are separated by 10 mm (W) by a dielectric material that is 1 mm thick (t). A = 100 mm x 1 mm = 100 mm^2. Length = 10 mm. If the resistivity for the dielectric material was 1000 Ω/mm, the resistance between the two electrodes would be 100 Ω.

Note: The concept of sheet resistance is applicable to electronic conduction. Ionic conduction is not necessarily linear and Ohms Law may not be applicable in this case.

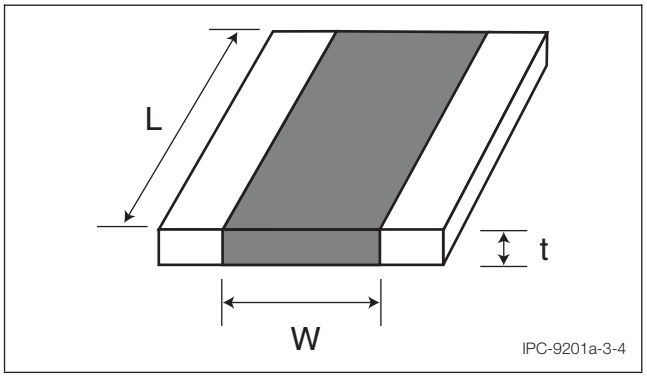

Figure 3-4 Sheet Resistance of a Thin Film (Gray Area Represents the Insulator)

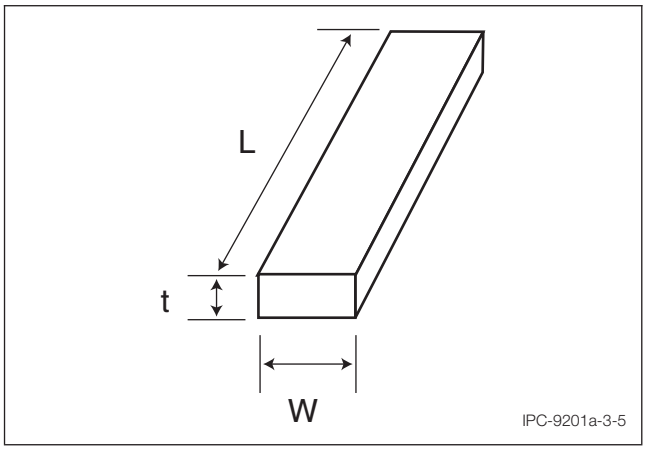

Figure 3-5 Resistance of a Metallic Conductor

3.2.2 A "Square" The concept of a "square" or normalization based on the number of "squares" is probably one of the most confusing aspects of SIR testing. It is related to the test electrode geometry, electrode separation, and substrate material. For an excellent coverage on this topic, the reader is referred to IPC-TP-831 (see Reference 1 in 10.1).

A "square" is not a cross sectional area, such as in^2 or cm^2. Two electrodes, each one inch long, separated by one inch, constitutes one square. Two electrodes, each one foot long, separated by one foot, constitutes one square, etc., as shown in Figure 3-6. The concept of squares is used to define a unit resistive element for a surface electrical pattern. This concept is based upon sheet resistance. Reference 1 in 10.1 explains this in greater detail.

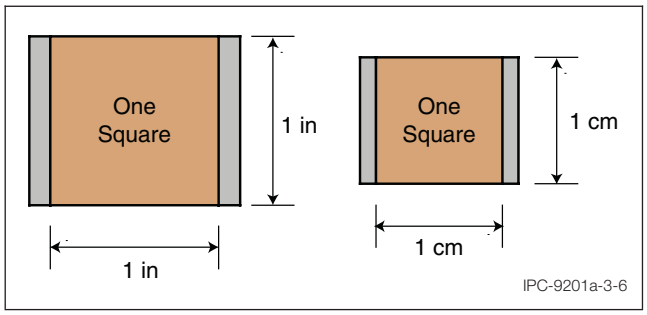

Figure 3-6 Concept of Squares

As noted in 3.2.1, the normalization may not be applicable to the precise interpretation of ionic conduction phenomena.

3.2.3 Series/Parallel Resistance Series resistance relates to the passage of electrical current through a series of resistances. The total resistance experienced is equal to the sum of the individual resistances encountered between high and low electrical potentials as shown in Figure 3-7. Parallel resistance refers to electrical current passing between high and low electrical potential by simultaneously passing through resistive elements which are not in series with each other as shown in Figure 3-8. The total resistance is the inverse of the sum of the reciprocal resistances.

$$R_{series} = R_1 + R_2 + R_3$$

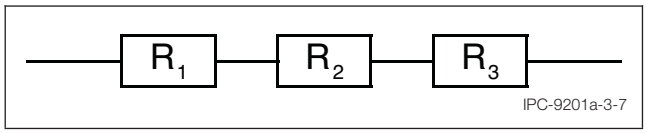

Figure 3-7 Total Resistance

$$1 / R_{parallel} = (1/R_1) + (1/R_2) + 1/R_3)$$

If we assume that R1 = R2 = R3, etc, then

R individual = (n) * R measured, where n = the number of squares

$$R_{parallel} = 1 / \text{Sum of Reciprocals}$$

3.2.4 Ohms Per Square Consider the separating spaces in an SIR test pattern to be "blocks" of unknown resistances, as in the Y-pattern illustration in Figure 3-9. The left-side portion of the pattern, where the separation is

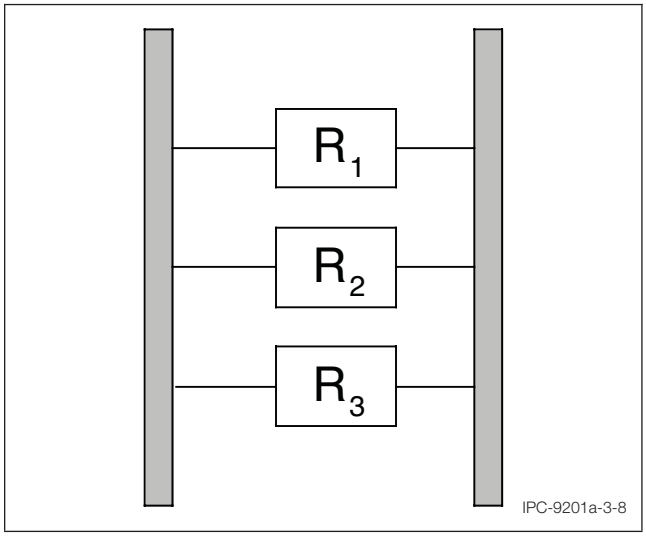

Figure 3-8 Parallel Resistance

greater than the 0.635 mm [0.025 in], is generally not included in the calculation of the number of squares. This pattern has 120 squares (see 3.2.4.1) or 120 blocks of unknown resistance, all assumed to be of equal value.

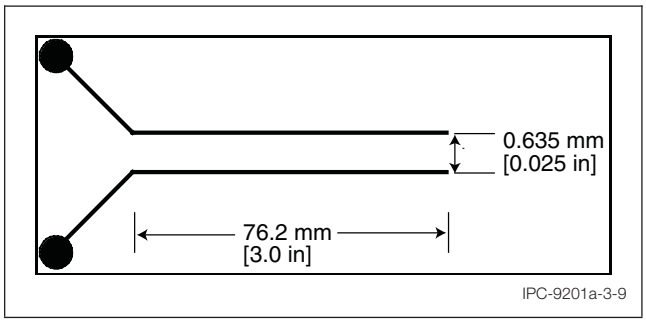

Figure 3-9 "Y" Pattern for SIR Testing

With a measured resistance of 100 megohms, then the individual unknown resistances must be 12,000 megohms (using the formula for the sum of parallel resistors and solving for R_x).

Ohms Per Square is an expression of normalized resistance. Since each "square" is a dimensionless unit, normalization of resistance data to an ohms per square value theoretically makes the data independent of electrode configuration/geometry, for electronic conduction.

The conversion of data to ohms per square has the underlying assumption that contamination is uniform across the entire test pattern, or that there is homogenous material at all points on the test patterns. Such an assumption might be the case when studying sheets of insulators or some other homogenous material, but the theory tends to fall apart when contamination is not uniform. An example might be a small spot of flux residue on a 3000 square pattern. Since electricity takes the path of least resistance, the leakage currents would flow through few squares containing the

flux residue, "ignoring" the other squares. Such an event violates the homogeneity assumption.

This is why the normalization of resistance to an ohms per square value is a questionable practice. There is the question of whether the contamination being studied is uniform or homogeneous. IPC round robin test programs have shown that the normalization is often a "hit or miss" proposition.

Example 1: Figure 3-10 illustrates a demonstration of the influence of varying amounts of flux residue that may be present on a circuit.

This shows the influence of different levels of flux on the SIR of a coupon as temperature rises under humid conditions. As would be expected, the lower the amount of flux residue, the less influence there is to the measured SIR. For example, in running a comparison of 6 ml of flux residue vs. 15 ml or 30 ml it can be seen that the SIR value drops dramatically with the larger amount of residue as the temperature and humidity increase until they reach a point where the residue reaches a volatilization temperature and starts to depart from the printed board, thereby permitting the SIR value to "improve."

Note also that this shows the volatilization of the flux residues as the temperture rises.

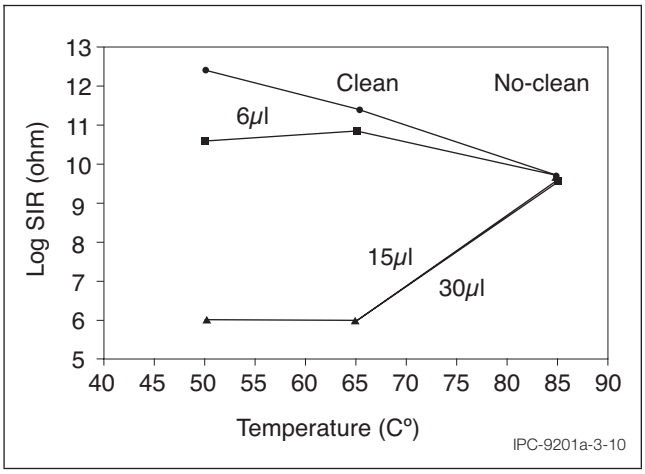

Figure 3-10 Influence of Flux Residue on a Circuit

Example 2: Within Figure 3-11 can be seen the scatter of results according to the coupon (pattern) design and the voltage gradient employed during the test. The figure shows that there is a strong dependence on the number of squares in the pattern, i.e., the gap between the tracks, and also on the applied voltage. With a lower voltage the SIR is lower, and with a higher voltage the SIR is higher. The control data is for a clean printed board, and here the results are independent of voltage. Hence it is more difficult to pass an SIR test with a lower voltage and a higher number of squares.

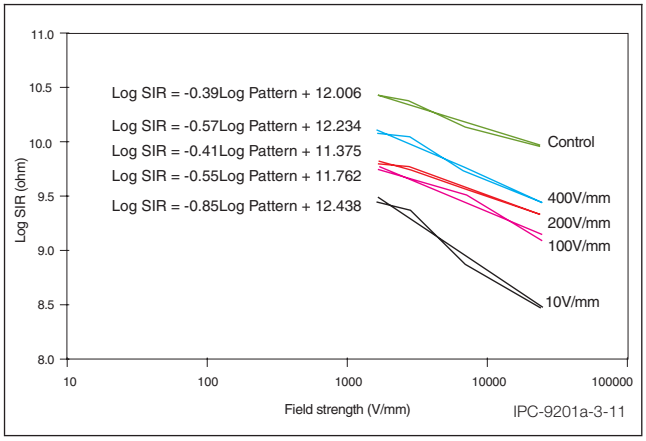

Figure 3-11 Scatter Results Based on Number of Squares

3.2.4.1 Examples of Square Count Calculations A wide variety of SIR test patterns can be found in Appendix C of this document.

1) The Military Y Pattern

Consider the standard military Y-pattern shown in Figure 3-9 used for quality conformance. The length of opposing conductor face is 76.2 mm [3.00 in]. It is not necessary to count the length of both faces, only the common area.

The separation is 0.635 mm [0.025 in]. Therefore, the number of squares would be: 76.2 mm/0.635 mm [3.00 in/0.025 in] = 120 squares.

2) Simple Comb Pattern

Consider the simple comb pattern shown in Figure 3-12. The area of interlap is denoted by the shaded area. The overlapping area is 25.4 mm [1.00 in] in height. There are 16 sets of common overlap. Therefore, the total circuit length of opposing faces is 16 * 25.4 mm = 406 mm [16 * 1.00 in = 16.00 in]. The spacing for all segments is 0.635 mm [0.025 in]. The number of squares would be: 406 mm/0.635 mm [16.00 in/0.025 in] = 640 squares.

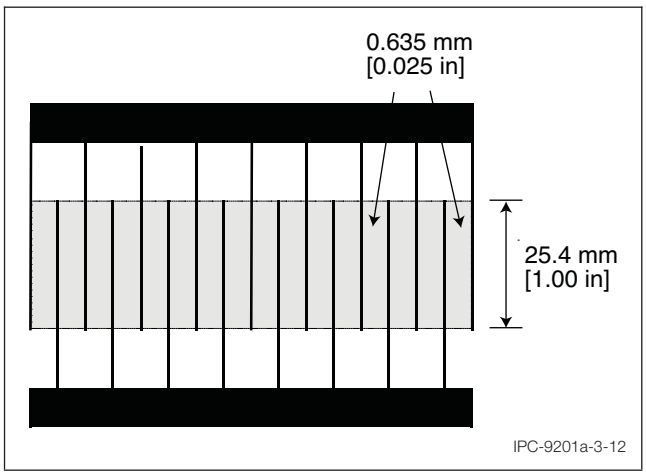

Figure 3-12 Example of a Simple Comb Pattern

For reference, the IPC-B-36 board comb patterns have a circuit length of 546 mm [21.5 in] and a spacing of 0.152 mm [0.006 in], for a nominal square count of 3583 squares. The IPC-B-24 board comb pattern has a circuit length of 518 mm [20.4 in] and a spacing of 0.508 mm [0.020 in], for a nominal square count of 1020 squares. The Bellcore pattern has a circuit length of 559 mm [22.0 in] and a spacing of 1.27 mm [0.050 in], for a nominal square count of 440 squares.

3) Interdigitated Mounting Pads

The third most common SIR pattern is interdigitated surface mounting pads as shown in Figure 3-13. Every other pad is grounded and you measure the SIR between pads for the whole set of pads. In this example, the individual pads are 1.27 mm [0.050 in] long and the spacing is 0.635 mm [0.025 in]. The amount of overlapping circuitry is 1.27 mm [0.050 in] * (16 overlap sites) = 20.32 mm [0.8 in]. The total number of squares would be 20.32 mm/0.635 mm [0.8 in/0.025 in] = 32 squares.

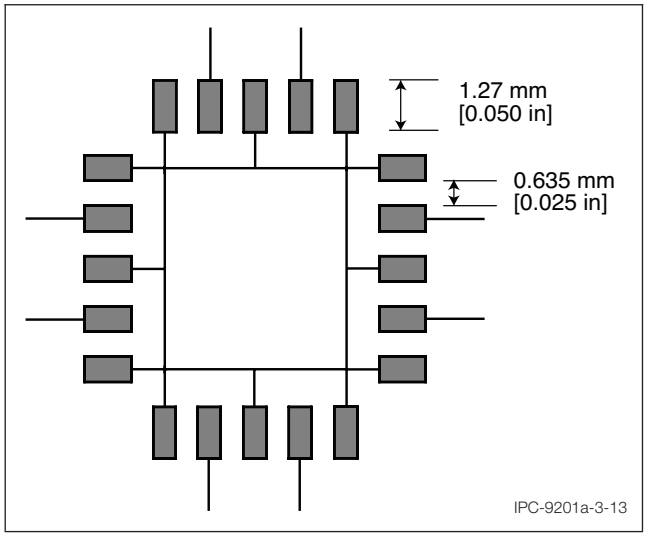

Figure 3-13 Interdigitated Surface Mount Pad

3.2.4.2 Use of Squares Information If the conversion of measured resistance to a normalized ohms per square is a questionable practice, as proposed earlier, why include it in this document?

Many technical specifications refer to the square counts of various patterns. The Bellcore TR-NWT-000078, for example, allows the use of an alternative SIR test pattern, provided that the alternative pattern has a squares count comparable or greater than the Bellcore pattern. Test reports (e.g., IPC-TR-580) sometimes list normalized data. So an explanation of squares and normalization was deemed appropriate.

Designers may ask the question of how large to design a test pattern, or how many ''squares'' to design into a pattern. The higher the square count of the pattern, the more sensitive the pattern will be to contamination. Going above 4500-5000 squares may make an SIR pattern too sensitive, and processes would have a difficult time passing using the historical pass fail levels found in IPC J-STD-004 or comparable military test standards. Going too low in squares count would lead to a situation which would pass except in cases of the grossest contamination.

Compare the comb patterns of the IPC-B-36 board (0.152 mm [0.006 in] lines and spaces, 3500 squares) with the comb patterns of the IPC-B-24 board (0.406 mm [0.016 in] lines, 0.51 mm [0.020 in] spaces, 1020 squares). In terms of board real estate area, the IPC-B-36 combs are smaller and more compact. The fine spacing (0.152 mm [0.006 in]) makes the comb very sensitive to contamination, but the compact size takes up a smaller area and so there may be a lower incidence of contamination. On the other hand, the IPC-B-24 is physically larger, offering more opportunity for contamination failures, but is not as sensitive.

3.2.5 Conduction Mechanisms The reader is encouraged to locate a good text from chemical engineering and read the sections on the dynamics of chemical transport.

In general, pure water is a poor conductor. As water becomes loaded with ionic materials, it becomes an electrolytic solution. The negatively charged anions and the positively charged cations serve to conduct electricity through the solution. The greater the level of ionic material present, the more current the solution is capable of carrying.

Deionized water is a very ''hungry'' solvent. It is desperate to pick up ions. Pure DI water (>10 megohm-cm and especially 18 megohm-cm) is corrosive in nature due to this fact. That is why metal piping cannot be used in DI water delivery systems, as it corrodes away. See Reference 6 in 10.1 for more details on DI water piping. Clean water, even if ''deionized'' will dissociate to some extent such that H^+ and OH^- ions will be present, though at very low levels.

3.3 Test Factors Affecting Results As indicated before, a tremendous number of factors can influence the results of an SIR test. Factors include materials parameters, the manner in which the samples were processed, how they were prepared for testing, etc. This section will deal with the factors related to testing setups and techniques.

3.3.1 Wiring The type of wire, wire insulation, wire attachment method, and wire positioning can and does affect test results especially when measuring at resistance levels greater than 10^{11} Ohms required by the latest specifications.

Types of wire can include solid or stranded wire, flat ribbon cable, standard single insulated wire, and shielded or unshielded coax cable. Some THB test setups use a smaller gauge wire (24-28 gauge) in order to fit more wires

through a cable port. Solid wire is more susceptible to breaking than stranded wire, but stranded wire can draw contaminants up under the insulation by capillary action.

The presence of some sort of shielding on the wire, such as with coaxial cable, can greatly decrease the amount of electrical noise in the measurements, but adds bulk to the setup. If coaxial cable is used, the shielding braid should be used only for grounding and must not be used to energize the test patterns or for routing the return current.

Wire insulation can be almost any polymer from polyethylene to polytetrafluoroethylene (PTFE). For SIR/THB testing, the insulation used should have a high dielectric strength, high insulation resistance, and should be halide-free. Polyethylene is typically inexpensive but has a lower resistivity than a PTFE, and is unsuitable at temperatures exceeding 50 °C. PTFE has excellent dielectric and insulating characteristics, such as low capacitance and dielectric constant, but is expensive, soft, and susceptible to damage and ''cold flow.'' PTFE is usually the preferred material for most THB testing. PVC (a halide-bearing polymer), or other low grade polymers, should be avoided. These low grade polymers often degrade quickly under the elevated conditions of SIR testing, outgassing chloride and resulting in unacceptable leakage currents.

Wire attachment can be by soldering, crimped connection, alligator clips, edge card connectors, or spring loaded probes. Each has their advantages and disadvantages. Soldering (hardwiring) provides the most reliable connection, but also introduces contaminants (flux) into the test sample. If a failure occurs, was it due to the material system or the contaminants from the soldering? It should be noted that soldering should not be done inside of a test chamber to avoid contamination of the chamber.

Crimped connections are reliable, but are only good for one test, after which they must be discarded and the wires refitted with connectors. There are also very few crimped connectors for SIR testing and a wide range of test assembly configurations. Alligator clips would have to be passivated, either by gold or nickel plating. They may also fall off the test board during testing due to chamber vibration. A permanent fixture using spring loaded, gold-plated pins is reusable and noncontaminating, but is very costly to make and is cost effective only for larger volumes of a set board design.

Edge card connectors have the advantage of multiple uses, ease of test sample connection, and limited possibility of contamination. However, the test substrate must be designed for edge card contact fingers and connectors can often provide a path for leakage currents between contact fingers. Another disadvantage of edge-card connectors is the potential for oxide formation and the loss of contact (spring) pressure over time. For this reason, the connector fingers must be gold plated and periodically checked for open circuits (loss of contact pressure).

The immobilization of the wiring is important. As a dielectric material flexes, small currents are generated (triboelectric currents) from the stresses induced within the insulation material. Also, the rubbing of insulating materials against each other may generate an electrostatic charge. Because SIR measurements are often in the picoampere range, these triboelectric and electrostatic currents can skew the results. Even vibration of the wiring, as might be caused by a running chamber, can generate such currents. By fixing the wires in place, both relative to each other and relative to the chamber, these currents can be minimized.

3.3.3 Sample Orientation in the Chamber During exposure to elevated temperature and humidity, a test electrode, together with the dielectric material, will function as a capacitor. The capacitance is dependent upon the humidity absorption of the dielectric at any particular time. If the test boards are placed perpendicular to the chamber air flow, the humid air will directly impact the test specimen, increasing water permeation. Wind speed, direction, turbulence all affect the consistency of the RH in the chamber and so affect absorption. Since most air flow in a chamber also is from the humidity generator, where humidity is 100% towards the front of the chamber, where it is not, there will exist a wet wind as a forcing function. The less direct the impact of the blowing humid air, the less the direct absorption. This effect is more pronounced in uncoated test boards. If the test samples are placed parallel to the air flow, the permeation impact is decreased. Parallel samples also decrease the turbulence of the air, allowing the chamber greater control of temperature and humidity.

The orientation of the test boards should always be vertical as shown in Figure 3-14. This decreases the chance that water condensing on an upper surface of a chamber will drop onto the test patterns. If edge card connectors are being used, the cards should be suspended under the connectors to prevent accumulation of water or contaminants. If wires are soldered or crimped to the test boards, the wires should hang under the test sample, such that contaminant or condensed water will run down the wires away from the test boards.

3.3.4 Voltage The test voltages applied will often affect the levels of resistance observed. If a low level of voltage is used as the forcing function, the resulting currents are smaller and therefore more susceptible to noise and are consequently less stable. If a high level of voltage is used, especially on a pattern with narrow spacings, the voltage could exceed the dielectric strength of the material, causing arcing, corona, and sample carbonizing.

Figure 3-14 Example of Test Coupons Using A Rack System Mounted Inside the Test Chamber (Picture courtesy of Concoat Systems Limited)

The usage of an electrical potential, and the associated levels, is often determined by commercial or military specifications. Historically, due to large circuit separations and insensitive instruments, bias voltages were typically 100 - 500 volts DC. Electrification voltages ranged from 500 - 1000 volts DC. As printed board circuitry becomes denser, a test pattern, which is usually tied to the typical spacings of the manufactured assembly, will have smaller circuit separations. Present day bias voltages range from 10 -100 volts DC. Electrification voltages are 10 - 500 volts DC. Reference two outlines testing which showed that the decreased electrification voltages have not led to unstable resistance measurements. Typically, test specifications lag technology by several years, which can lead to electrical overstress.

Most electrical potentials used in THB testing have historically been direct current (DC) potentials. More recent experimentation has started to include the use of alternating current (AC). The usage of AC or DC depends on what failure mechanism is being tested for. A DC voltage is used to show failures by electrochemical and current leakage. An AC voltage is often used if the assembly is designed for AC functionality, or if the failure mechanism is expected to be failure of the dielectric material.

The voltage applied to test patterns affects the dendritic filament growth rates as shown in Figure 3-2. The quantity of metal deposited by electrolysis is proportional to the current carried by the metal ions. However, only a part of the current flow in the thin absorbed water film is due to such ions. Hydrogen ions are also present and there may be contributions from other conduction mechanisms (see Reference 12 and Reference 13 in 10.1). Hence the relationship between applied voltage and filament growth rate is not a simple one. Experimental work suggests that a half-power law applies - raising the voltage by 10x gives a 3x increase in filament growth rate.

3.3.4.1 High Voltage Testing Assemblies exist which have electrical potentials of thousands of volts between conductors. Such an assembly may be a high voltage power supply, or X-ray equipment. Low voltage testing, on the order of 50-100 volts, may be insufficient to detect fault mechanisms such as dielectric breakdown, which would occur at the higher voltages experienced in service.

Several precautions are required to get good results from high voltage tests. First, care must be taken to limit the energy of the breakdown arc. This can be done with standard circuits. If the energy is not limited, the board can be damaged (carbonized) by the arc. Second, dust and other debris can easily give false failures. If a breakdown occurs, carefully clean the board and then retest to assure that the failure is not a spurious result. Third, the test is easily confused by surface flashover. At 1000 volts, a surface arc will jump 0.254 - 0.38 mm [0.010 - 0.015 in] if the surface is smooth. This is further than air breakdown and arises because of a phenomena known as ‘‘dielectric enhanced breakdown.’’ Such a condition often occurs when solder mask coverage is incomplete. Above 1000 volts, false failures from surface flashovers in the test fixture limits the utility of the test.

The disadvantage of high voltage testing is cost and speed. Generally, test sets capable of high voltage are costly. Standard semiconductor switching will not work and either high-power relays or special semiconductors are required. Capacitance and inductance effects also limit the rate of testing. The higher the voltage, the slower the test.

When properly done, high voltage testing is a good way to assure reliability for high voltage operation. However, it adds cost and should only be done where required by the end use of the circuit. As a practical matter, the test should be limited to 1000 volts DC. See Reference 5 in 10.1 for additional information on high voltage testing.

3.3.5 Test Temperature The test temperature can affect many factors, including the amount of water vapor in the air, the ionic mobility of electrolytic solutions, the rate at which plasticisers leave the printed board, etc. Historically, the ‘‘aging’’ of a printed board assembly was thought to follow an ‘‘Arrhenius’’ reaction rate, whereby every 10 degrees Celsius rise in temperature would double the aging rate.

Example: One year of tropical service (35 °C, 85% RH) could be approximated by 6 months exposure to 45 °C, 85% RH, three months at 55 °C, 85% RH, etc.

This hypothetical aging rate grew out of thermal aging studies using dry heat. It is unknown whether the humidity has a synergistic effect on the aging rate; but without humidity, many of the electrochemical reactions would not take place.

It should be noted that many contaminant materials which influence SIR levels may be removed from the test substrate at elevated temperatures, either through sublimation or evaporation of the contaminant. Conformal coating of samples will hinder such a loss of contaminant materials, hence coating over flux (no-clean) residues may actually exacerbate a problem rather than resolve it.

3.3.6 Test Humidity The test humidity affects the amount of water vapor present to produce electrolytic solutions with contaminants on a board surface. A low level of relative humidity in a test will generally not lead to electrochemical migration phenomena, whereas a high level of relative humidity will saturate a printed board, leading to more cases of electrochemical migration.

3.3.7 Rate of Change, Ambient to Elevated Most TH/THB testing requires a conditioning period at ambient conditions, prior to initial measurements. This conditioning period is based in part on ASTM measurement practices. In many cases, test samples may be stored in sealed containers, such as heat sealable bags. If processing fluids (such as water from aqueous cleaning) were entrapped with the test samples, it is desired that the test sample be allowed to equilibrate to a standard environment.

Following initial measurements, the test conditions must be changed from ambient to elevated conditions. The rate at which this change takes place can cause condensation on a test board, especially if the board has a large thermal mass. As the chamber heats up, the heating of the test specimens will lag behind the moisture laden air of the chamber (usually steam). If there is a great enough temperature difference between the test boards and the air, condensation can occur. Consider a cold can of beer on a hot summer day. Water condenses on the cold surface of the can from the surrounding atmosphere. In most specifications, the presence of condensed water on uncoated test patterns will invalidate the test.

The rate of change from elevated conditions to ambient conditions does not have this condensation effect as the test parts are usually hotter than the surrounding air, eliminating the chance for moisture condensation.

3.3.8 Test Board Design Many factors related to the layout of the test patterns on a printed board can affect the test results. These include: line spacing, physical geometry of the test patterns, routing of the lands from test patterns to contact fingers, physical spacing of voltage application lines and current return lines, physical size of the test board, presence of guard traces, and surface topography of the laminate.

The latest specification revisions recommend the use of coupons that have been specifically designed to accommodate most if not all of the issues that are presented below and Appendix C contains a discussion on the strengths and weaknesses of available test vehicles.

a) Line Spacing This is the separation between electrodes. The spacing between electrodes will determine the maximum amount of voltage that can be applied to a test pattern. The maximum voltage should not exceed the dielectric strength (expressed in volts/mil) of the laminate material. IPC-6012 has requirements on the maximum allowable voltage based on dielectric strength. If the purpose of the testing is to critique production, the line spacings on a test pattern should be representative of the minimum spacing of circuitry on production boards.

On the other hand, test boards used for wave solder evaluations should incorporate the minimum line widths and spacings not protected by solder mask to prevent bridging problems. If solder paste evaluations are being performed, stencils must be available for the test boards. Since it is rare that solder paste is applied to conductors (on production boards), printed board designs will have to consider spacings from land to land.

For a given applied electrical potential, increasing the conductor spacing will increase the series resistance, thereby reducing the voltage gradient and reducing the current available for metal deposition and filament growth.

b) Physical Geometry of the Test Patterns Electromagnetic energy tends to concentrate at points or right angles. Test patterns having square corners or sharp points on the electrodes will generally have electrochemical migration initiate at these areas. Test pattern electrodes should have rounded corners wherever possible. Poor etching during printed board fabrication can lead to sharp points and produce the same effect.

Figure 3-15 shows the design of interdigitated combs terminations. It also shows the growth of dendrites resulting from an SIR test and using back-lighting to the coupon.

If the test pattern is large, such as a large comb (many interdigitated spaces), the pattern can act as both a capacitor and as an antenna, leading to dielectric charging and to electromagnetic interference, respectively.

c) Routing of the Lands If the land used to energize the test pattern is adjacent to the land used to return the current from the test pattern, cross-talk and leakage currents can arise, skewing the measurement. Measurement of the resistance should be across the target electrical pattern and not across the adjacent traces leading

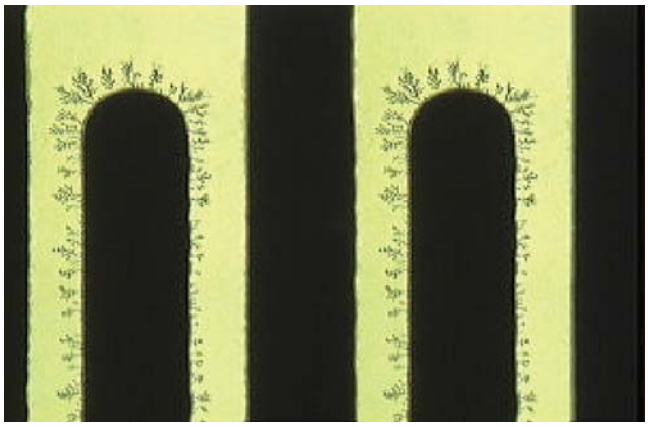

Figure 3-15 An Example of Dendrite Growth

to the electrical test patterns. In practice, the routing of the voltage supply lands and the current-return lands should be separated as widely as possible, with intervening guard traces if possible. Care should be taken not to route the cathode supply line from pattern #1 along the anode supply line of pattern #2. This can cause errors if multiple patterns are being measured simultaneously.

d) Guard Traces This is one of the most important elements in designing and placing SIR circuitry. Guard traces are circuit lands used to isolate voltage-supply and current-return lands on a test board. In most cases, the guard traces are placed at a potential similar to the signal trace (often ground), and prevent leakage currents from entering the test measurements. In most cases, the voltage ''leaking'' from the voltage-supply traces to the guard traces does not significantly affect the test measurements. The use of guard traces ensures the measuring of resistance where it is intended, and not at some extraneous location. If in doubt, guard it.

e) Physical Size of the Test Board The size of the test board can affect the stability of readings. A small test board may respond more quickly to changes in temperature and humidity due to its lower thermal mass. Smaller boards are therefore more sensitive, but less stable. The reverse is true for larger boards.

f) Location of the Test Patterns SIR test patterns are of little utility if they are far away from the contamination effects you wish to examine, or do not represent the challenges to cleaning. For this reason, SIR patterns are typically placed in some of the following areas:

- Under large footprint devices. Comb patterns or parallel traces under a large device, such as an LCC or ASIC, can show the effects of entrapped flux in an area that is difficult to clean, or that is shielded from various process effects (e.g., spray cleaning that cannot penetrate under the device).
- Within the perimeter of a large component. If you had a 256 I/O ASIC device, mounted to surface mount pads, you could run a parallel set of traces around the inner perimeter of the footprint area. This would determine effects from reflowed solder paste flux, which may be forced back under the device during reflow.

Figure 3-16 and Figure 3-17 depict test boards designed with these concepts.

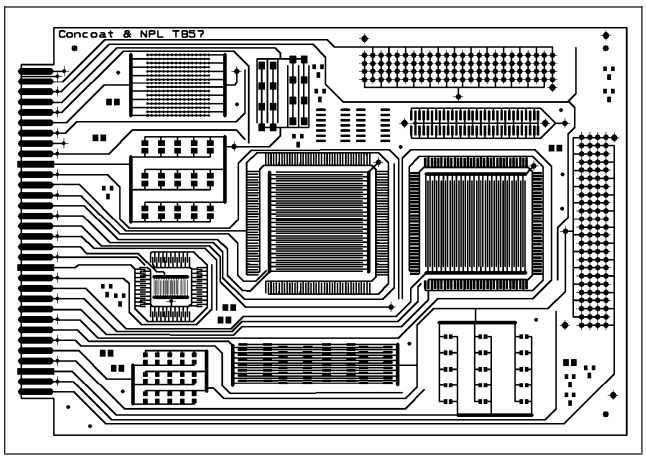

Figure 3-16 The IEC Process Characterisation Test Coupon/Vehicle (From IEC 61189-5)

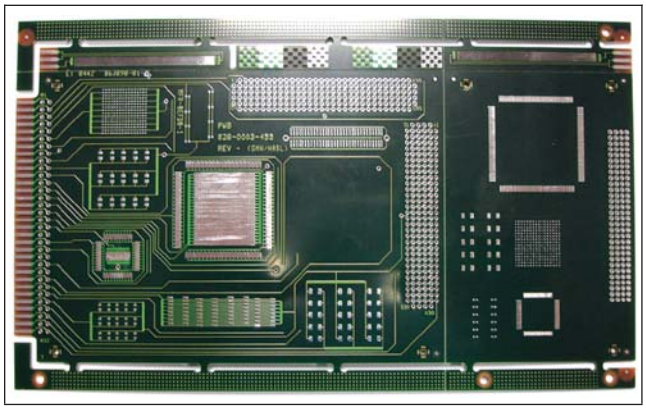

Figure 3-17 An IPC-B-52 Test Coupon/Vehicle Designed by the SIR TG

g) Dummy Components The presence of components on an assembly will, most likely, result in a greater concentration of trapped residues, especially when considering wave soldering techniques. For this and other process characterization tests, the use of dummy components is both useful and advisable.

It is essential that such dummy components be true ''dummy'' and not ''scrap'' devices. If a ''scrap'' device is used, the internal conductors and connections will certainly affect your test results; in accordance with Sod's (Murphy's) law, probably in a bad way.

3.3.9 Frequency of Measurement Historically, resistance measurements in an SIR test were made at set times, such as every 24 hours, or five times in a seven day period. Recent research and advances in SIR equipment design

have indicated that frequent monitoring of SIR levels may be the only way to catch electrochemical migration events during the testing. With frequent monitoring, it is possible to obtain a measurement for a test pattern every five minutes, as opposed to every 24 hours where valuable data as can be seen in Figure 3-18 may be lost. The use of frequent monitoring techniques is therefore strongly encouraged.

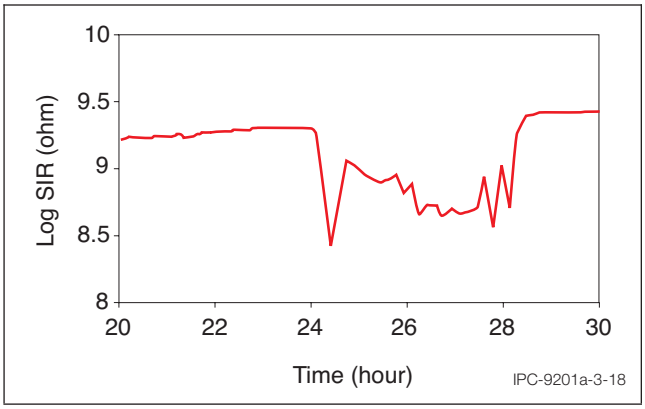

Figure 3-18 Temporary Reduction in SIR That Would be Missed by Infrequent Testing

3.3.10 Conformal Coating Some specifications require SIR testing on conformally coated samples. In general, conformal coating will limit any interactions between the humid test environment and the test patterns under the coating. The overall effect is a delayed reaction. Conformal coatings represent a physical barrier, but no conformal coating will keep water out indefinitely. Conformal coatings are all organic materials with water permeability coefficients. Conformally coated samples are often tested in a cyclical environment that promotes water condensation. The cycling of temperature causes a ''pumping'' action for water vapor. Longer testing (relative to an uncoated sample) may be needed for water vapor to interact with processing residues in order to initiate failure mechanisms.

3.4 Known Process Effects on SIR Levels Good SIR performance is related to high levels of cleanliness in the test sample. The ability to remove cleaning agents and other process residues is critical to achieving high SIR levels. If ionic contamination is not removed, it can become entrapped in ensuing operations, leading to lower SIR levels. There are also nonionic residues that can influence SIR, notably glycol and silicone surfactants that are commonly used in permanent solder masks and solder fluxes.

3.4.1 Precleaning If test substrates are precleaned prior to sample processing, the SIR levels generated will be attributable to the sample processing and not some preexisting contamination. Several precleaning methods are possible: pumice scrubbing with a brush and good rinsing, a chemical micro-etch, solvent cleaning, and/or aqueous cleaning. A final wash with isopropanol/water is recommended for any precleaning method. Running the samples through a bulk ionic contamination tester serves this purpose well. Samples should be thoroughly dried before being exposed to the test process or before SIR testing.

3.4.2 Developing Process Effects The method by which solder masks are processed can affect the SIR levels.

- ***Developing vs. No Developing –*** Test coupons that are developed and rinsed will typically have SIR levels 0.5 - 1.0 decades higher than test coupons which have not been run through the developer.
- ***Developing Process —*** A longer exposure to the developer solution will decrease SIR levels, due to the extended chemical attack fo the developer chemicals. This effect appears to be independent of developer chemistry. The use of sodium carbonate, potassium carbonate, or monoethanolamine as the developer chemistry does not appear to have any effect on SIR levels.
- ***Rinsing after Developing —*** The efficiency of the rinsing operation is critical. Higher water temperatures (45 - 55 °C) and longer rinse times serve to increase SIR levels. The water quality is also important. Deionized water rinsing is preferred over tap water rinsing. An extended soak (two minutes, 65 - 70 °C) after developing has been shown to improve SIR levels. In general, the developing process adds ionic contamination which can decrease SIR levels. Removal of ionic contamination is critical for good SIR performance.
- ***Post-Curing –*** If post curing is part of the mask's recommended processing, it is essential for good SIR levels.

3.4.3 Curing Effects Curing laminates, solder masks, conformal coatings, etc., increases the cross-linking of the polymeric structures. As the degree of cross-linking increases, the higher the insulating characteristics of the material, resulting in higher SIR levels. Most cure mechanisms in the electronics industry involve either ultraviolet (UV) light curing, a thermal cure (bake), or a combination of the two. Increasing the UV exposure or the length of the bake will generally increase the amount of cross-linking.

3.4.4 Hot Air Solder Leveling (HASL) The HASL process is typically harsh, raising a laminate and solder mask above the glass transition temperature (T_g) while the surface is soaked with flux. The greater the efficiency of the post-HASL cleaning process, the higher the SIR numbers.

It is generally agreed that the tin-lead deposition process in printed board fabrication is one of the biggest factors in the degradation of SIR values. Both HASL and tin-lead plating/fusing are generally done with chloride-bearing or bromide-bearing fluids that are difficult to remove after the reflow operation. The tin lead deposition process can drop SIR numbers by 2-3 decades (10^{12} to 10^{9}). Reference 3 in 10.1 is the Bellcore qualification document. The SIR pass-fail numbers of that specification are lower for tin-lead